A 126μW Current-Reuse Telescopic OTA with Class-AB Output Stage

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***Abstract*—In this paper, a low-power two-stage fully differential operational transconductance amplifier (OTA) is presented. A current-reuse CMOS based cascode telescopic topology is implemented as the input stage for high-gain and low power consumption, while a Class AB amplifier is designed as the output stage to improve slew performance and reduce the overall power consumption. Furthermore, a common-mode feedback (CMFB) circuit is used to stabilize the output common-mode voltage level to 0.9V. Circuit parameters are optimized by a $\mathbf{g_m/I_d}$ based design flow in a 0.18μm manufacturing process. Simulation results show that the design achieves outstanding performance of 0.033% static settling error, 0.065% dynamic settling error, 38ns settling time, 272$\mu\mathbf{V}/\sqrt{\mathbf{Hz}}$ noise, and 126μW power consumption from a 1.8V power supply.**

***Index Terms*—operational transconductance amplifier (OTA), low power, current-reuse**

TABLE I: design specifications and result summary

		Specs	Our Results
Values for C_1, C_2, and C_L			500fF, 500fF, 1pF
Static settling error		≤ 0.1%	0.033%
Dynamic settling error		≤ 0.1%	0.065%
Output swing		[-1.2V, 1.2V]	[-1.706V, 1.706V]
Input common-mode range			[576.5mV, 900.1mV]
OTA open-loop DC small-signal gain (A_{dm})			75.6dB
Loop gain at low-frequency ($\beta \cdot A_{\mathrm{dm}}$)			69.36dB
Loop gain unity gain frequency			27.998MHz
Loop gain Phase margin		≥ 60°	60.557°
Settling time	Up	≤ 40ns	37.885ns
	Down	≤ 40ns	37.885ns
CMRR at DC		≥ 60dB	94.4dB
PSRR at DC		≥ 60dB	82.28dB
Total output noise		≤ 300μV	272μV
Power consumption			126μW

I. Introduction

In modern analog and mixed-signal (AMS) integrated circuit (IC) designs, metrics such as power consumption, noise, and frequency bandwidth are considered. Among these design factors, power consumption has gained higher and higher attention due to the rapidly expanding market of the Internet of Things (IoT) devices, wireless communication elements, and consumer electronics. Thus, minimum power consumption is paramount in analog IC design.

Operational transconductance amplifiers (OTA) often consume the highest portion of total power usage in a low-power analog circuit, and are also the bottleneck of circuit power optimization. To design a low-power OTA, several approaches have been proposed. A widely used method is biasing the transistors in sub-threshold region. The advantages of sub-threshold circuits are high intrinsic gain, large output swing, and very low supply voltage…etc. While the main disadvantage is that they have lower speed, which results in smaller transient frequency. Other techniques for reducing power consumption have also been proposed. Hogervorst *et. al* [1] demonstrates a Class AB output stage to reduce the quiescent current while preserving the signal. Song *et. al* [2] shows a current-reuse scheme by letting the current flow through two differential pair in order to reduce current while maintaining the same g_m/I_d value.

In this work, we present a low-power two-stage OTA [3] design. The first stage of the OTA contains a telescopic amplifier [4] with current-reuse technique to reduce the current consumption by half comparing with conventional cascode telescopic OTA. The second stage consists of a Class AB amplifier [5] and a miller compensation capacitor to improve the output swing and meet the frequency requirement. A common-mode feedback (CMFB) circuit [6] is adopted to stabilize the output common-mode voltage. Also, a power efficient biasing circuit is implemented to make sure all the transistors operate at desired region. Simulation results demonstrate that the design satisfies all the requirements, as shown in Table I.

The remaining sections are organized as follows. Section II introduces the structure of our design. Section III gives the derivation of design parameters. Section IV shows the simulation results, and Section V concludes this paper.

II. Circuit Topology

To minimize power consumption, the selection of the OTA topology is essential. In this section, we introduce the overall structure of our OTA design, and detail each sub-module of the circuit. Figure 1 shows the schematic design of the designed OTA. We can observe that a current-reuse telescopic amplifier is adopted as the input stage, and a Class AB amplifier is used as the output stage.

A. First-Stage Current-Reuse Telescopic Amplifier

Achieving high gain and low power consumption simultaneously is challenging. The small-signal gain of the conventional telescopic OTA design is $0.5 \cdot (g_m r_o)^2$, where g_m is the transconductance of the input transistor and r_o is the output resistance. Current-reuse telescopic OTA, however, can maintain the same magnitude of gain with smaller drain current I_d. Since the input port connects to both NMOS and PMOS, the gain of the current-reuse telescopic OTA shows as

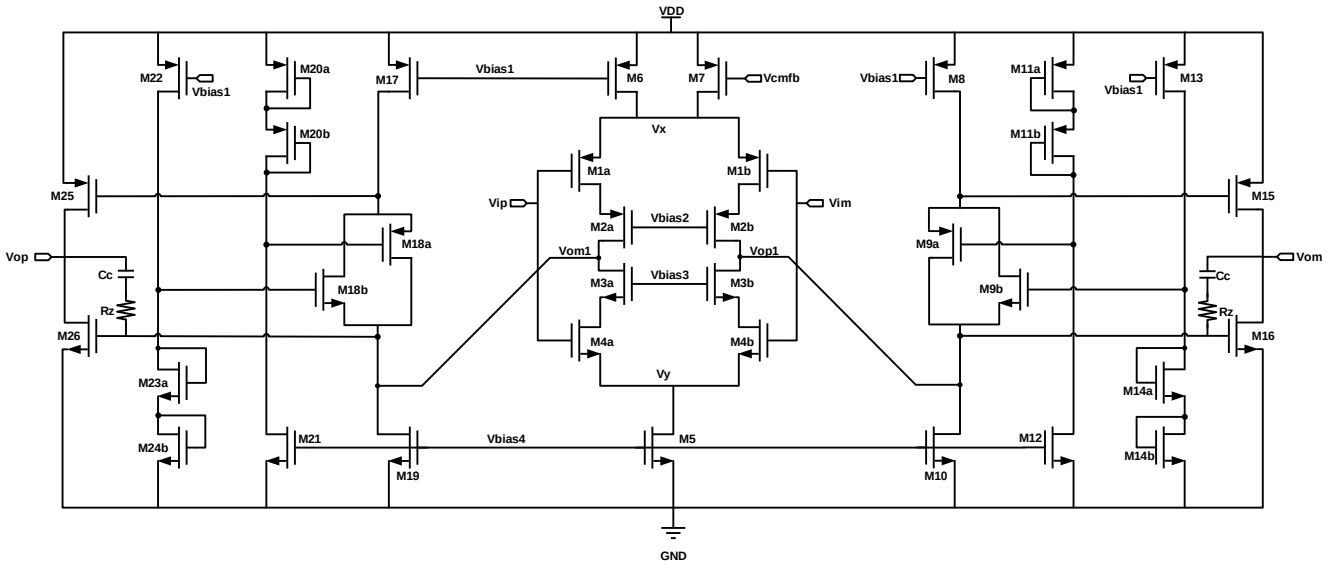

Fig. 1: Overall schematic of two-stage OTA design.

$((g_{\mathrm{mn4}} + g_{\mathrm{mp1}})r_o)^2$, where g_{mn4} is the transconductance of the NMOS M4a connected to the input port, and g_{mp1} is the transconductance of PMOS M1a.

Consider the current-reuse telescopic OTA schematic design in Figure 2 and assume that $g_{\mathrm{mp1}} = g_{\mathrm{mn4}}$. Therefore, the value of transconductance of each transistor becomes one-half the original value. Keeping the same g_m/I_d value, the current flowing through each transistor also be cut by half.

Despite the high gain and low power consumption, the telescopic OTA design still carry some deficiencies, e.g. restricted swings. Therefore, a second stage circuit is added to our topology to resolve the shortcomings stated above.

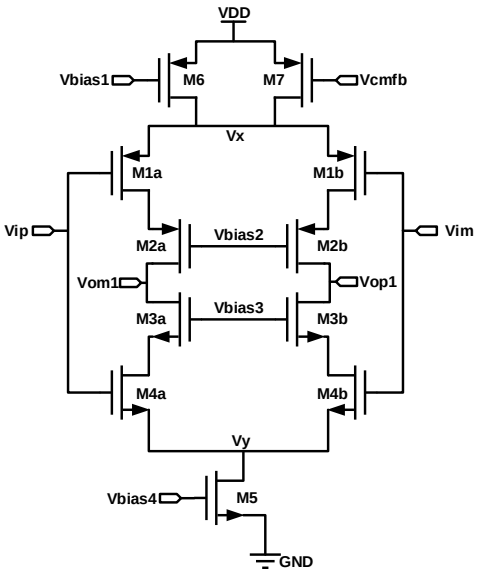

Fig. 2: Schematic of the current-reuse telescopic amplifier.

B. Second-Stage Class AB Amplifier

To satisfy the required output swings and further boost the overall gain value while keeping the current usage low, a Class AB amplifier is implemented as the second stage. The detailed structure of the second stage amplifier is shown in Figure 3.

When no differential input signal applied, both M15 and M16 is biased at a barely-on state, meaning that minimum current will be consumed while input signal is zero. In order to do this, the gate voltage of M15 is pushed to about $1.3\mathrm{V}$ and the gate voltage of M16 is pushed to about $0.5\mathrm{V}$ and the two diode-connected (M11a and M11b) are pushed to subthreshold region. Because of such biasing, the V_{ov} is low and thus, the output swing is higher than conventional common source output stage design. However, also because of such bias, the output node of the first stage has lower biasing point, around $0.5\mathrm{V}$, which put the pressure on lower side NMOSs biasing because of the limited voltage swing. This low common mode output will also lead to an unsymmetrical input common mode range, because when the input common-mode voltage is high, the bottom devices (M3, M4 and M5) are pushed to linear region.

Traditionally, for a common source output stage, the slew will be limited because the load transistors are not able to provide the required current. However, by using the designed Class-AB output stage, instantaneous current will can be provided and therefore, less current is need for slew requirement. The limitation of reducing the current further more is the stability requirement, since reducing the second stage current will reduce g_{m2} and reduce the non-dominant pole location.

C. Biasing Circuit

Biasing circuit is a critical sub-module that largely affects the overall performance of the OTA, and even determines if a OTA functions properly. In our design, a magic battery

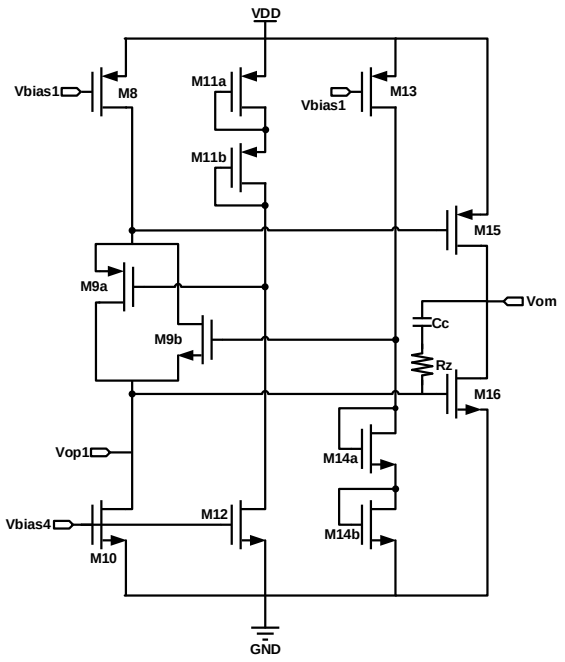

Fig. 3: Schematic of the Class AB amplifier.

approach [7] is chosen. The architecture of the biasing circuit is shown in Figure 4, while the other side of V_x and V_y is marked in Figure 3.

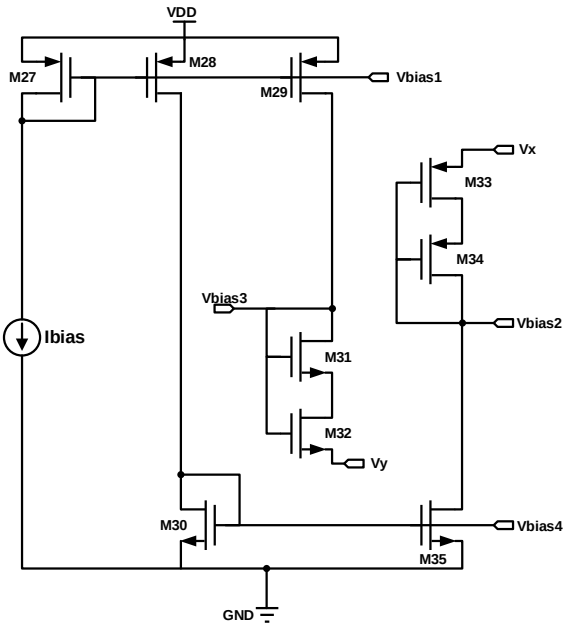

Fig. 4: Schematic of the biasing circuit.

D. Common-mode Feedback

Stabilizing the output common-mode voltage to the desired value ensures all the transistor work in desired region, such as saturation region for the first-stage and second-stage. A CMFB circuit compares the average voltage of two differential output ports and a user-defined desired output common-mode voltage, then feeds a signals (V_{cmfb}) back to control the tail current in the first stage telescopic OTA. R_1 and R_2 are used to averaging the differential signal (V_{op} and V_{om}) to common mode voltage (V_{oc}). Figure 5 shows the topology of the CMFB circuit. The desired common-mode circuit $V_{\mathrm{oc\_des}}$ is generated by two transistors (M39 and M40) instead of two large resistors in order to reduce the current flow. Because ensuring a stable common mode is essential in this design, a larger channel length is used to reduce process variation.

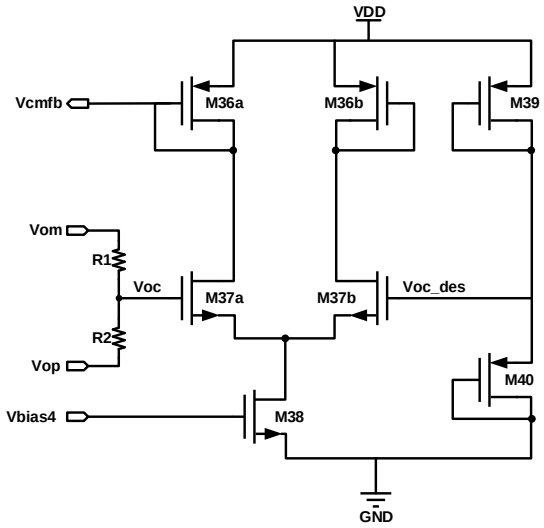

Fig. 5: Schematic of the CMFB circuit.

III. Circuit Parameters Derivation

Given the circuit topology, the next step is to derive the value of each design variable, e.g. width/length of each transistor, capacitors and resistors value. Detailed steps of variables derivation are described in this section. The exact value of design variables used in our OTA can be found in Appendix.

A. First-Stage Variables

Consider the dynamic settling error and settling time requirement, we have

$$\epsilon_d \leq 0.1\%,\ t_s \leq 40\mathrm{ns}, \tag{1}$$

where ϵ_d is the dynamic settling error and t_s is the settling time. Assume $t_s = t_{\mathrm{slew}} + t_{\mathrm{lln}}$, where t_{slew} is the slewing time and t_{lln} is the linear settling time. The Class AB structure in the second stage can provide instantaneous current. Therefore, we allocate t_{slew} and t_{lln} to $10\mathrm{ns}$ and $30\mathrm{ns}$ respectively, to relax the bandwidth requirement and reduce the current consumption.

To achieve $\epsilon_d \leq 0.1\%$, the equation

$$t_{\mathrm{lln}} \cdot \omega_c = 6.9 \tag{2}$$

should be satisfied [8], where ω_c is the loop gain unity gain bandwith, which is also equal to the close-loop bandwidth.

Given $t_{\mathrm{lln}} = 30\mathrm{ns}$, the value of ω_c is then calculated to be 2.3×10^8; thus, the loop gain unity gain frequency f_c is $36.6\mathrm{MHz}$.

To obtain the equivalent transconductance g_{m1} of the first stage amplifier, we have

$$g_{\mathrm{m1}} = \frac{\omega_c \cdot C_c}{\beta} \tag{3}$$

where C_c is the value of the compensation capacitance and β is the feedback factor.

$$\beta = \frac{C_f}{C_f + C_s + C_{\mathrm{gg1}}} \tag{4}$$

assuming C_{gg1} is negligible and $C_f = C_s = 500\mathrm{fF}$, β is about 0.5. In reality, C_{gg1} is not negligible. therefore, we assume that β is around 0.48. By setting C_c to $500\mathrm{fF}$, we have

$$g_{\mathrm{m1}} = g_{\mathrm{mn}} + g_{\mathrm{mp}} = 238\mu\mathrm{S}. \tag{5}$$

Assuming $g_{\mathrm{mn}} = g_{\mathrm{mp}}$; therefore, $g_{\mathrm{mn}} = g_{\mathrm{mp}} = 119\mu\mathrm{S}$. To achieve low power consumption, value of g_m/I_d for each transistor is set to $19\mu\mathrm{S}/\mu\mathrm{A}$, so that the drain current of each transistor should be $6\mu\mathrm{A}$. By current density chart, the channel width W_{n1} for NMOS transistors and the channel width W_{p1} for PMOS transistors turned out to be $2\mu m$ and $6\mu m$, respectively.

B. Second-Stage Variables

Given phase margin $PM = \tan^{-1}(\frac{\omega_{\mathrm{p2}}}{\omega_c})$ [9]. Consider the phase margin constraint $PM \geq 60°$, the value of non-dominant pole ω_{p2} should be manipulated. Let PM be 70°, we have $\omega_{\mathrm{p2}}/\omega_c = 2.8$. By equation

$$\omega_{\mathrm{p2}} \approx \frac{g_{\mathrm{m2}}}{\frac{C_{\mathrm{Ltot}}C_{\mathrm{gg2}}}{C_c} + C_{\mathrm{gg2}} + C_{\mathrm{Ltot}}}, \tag{6}$$

and the value of total load capacitance C_{Ltot}, parasitic capacitance of second stage input transistors C_{gg2}, and compensation capacitance C_c already defined, we have $g_{\mathrm{m2}} = 3\mathrm{mS}$. Assume $g_m/I_d = 17\mu\mathrm{S}/\mu\mathrm{A}$ for each transistor, the drain current is decided to be $176\mu\mathrm{A}$. By current density chart with channel length equals to $0.18\mathrm{n}m$, the channel width W_{n2} and W_{p2} of second stage NMOS and PMOS transistors are set to $25\mu m$ and $65\mu m$ respectively. However, because of the Class-AB technique, second stage current is greatly reduce by biasing the transistor at barely-on state. The final output stage current is around $22\mu\mathrm{A}$ while satisfying the stability requirement.

C. CMFB Circuit

The most important part of the CMFB loop is the size ratio of the tail current source of the telescopic amplifier M6 and the feedback transistor M7, as shown in Figure 1. If the size of transistor M7 is too small, the feedback current would become insignificant, thus unable to stabilize the feedback loop and sustain the output common-mode voltage. By heuristic, the size ratio of the two transistors (M6 and M7) are often decided to be $0.7 : 0.3$.

IV. Simulation Results

The simulations are conducted with $0.18\mu m$ CMOS manufacturing process in Cadence ADE environment. The execution temperature is set to $27°\mathrm{C}$ and the supply voltage is $1.8\mathrm{V}$. DC sweep, DC analysis, stability analysis, AC analysis, transient analysis, and noise analysis are included in our simulation process. Figures of the simulation results are presented in Appendix.

A. DC Sweep

This simulation derives the relation between differential-mode gain and output swing, and the waveform of output common-mode voltage versus differential-mode gain, as shown in Figure 10 and Figure 11.

B. DC Analysis

To evaluate the power dissipation of our design, DC analysis is performed. The total current usage and the power supply voltage of our design are $70\mu\mathrm{A}$ and $1.8\mathrm{V}$ respectively. Hence we have total power dissipation $P = I \cdot V = 126\mu\mathrm{W}$. Figure 12 shows the power consumption result.

C. Stability Analysis

As for phase margin and unity gain frequency, we execute stability analysis. Figure 14 presents the curve of loop gain and phase margin of our design w.r.t frequency. Note that the final phase margin is $60.557°$ and the unity gain frequency is about $28\mathrm{MHz}$.

D. AC Analysis

By running AC simulation, we have the CMRR and PSRR results, as shown in Figure 15(a) and Figure 15(b). The frequency response of the OTA is shown in Figure 16.

E. Transient Analysis

Transient simulation gives the data of static settling error, dynamic settling error, and settling time. Figure 17 and Figure 18 show the results of going up and going down settling.

F. Noise Analysis

Figure 19 shows the noise summary of our OTA, the final noise turn out to be $272\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$.

V. Conclusion

This work presents a low-power fully differential two-stage OTA design with a current-reuse telescopic first stage and a Class AB second stage, which outperforms all the design specifications. According to simulation results, the proposed OTA achieves 0.033% static settling error, 0.065% dynamic settling error, $38\mathrm{ns}$ settling time, $272\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ noise, and an excellent power consumption of $126\mu\mathrm{W}$ for $1.8\mathrm{V}$ power supply,

ACKNOWLEDGEMENT

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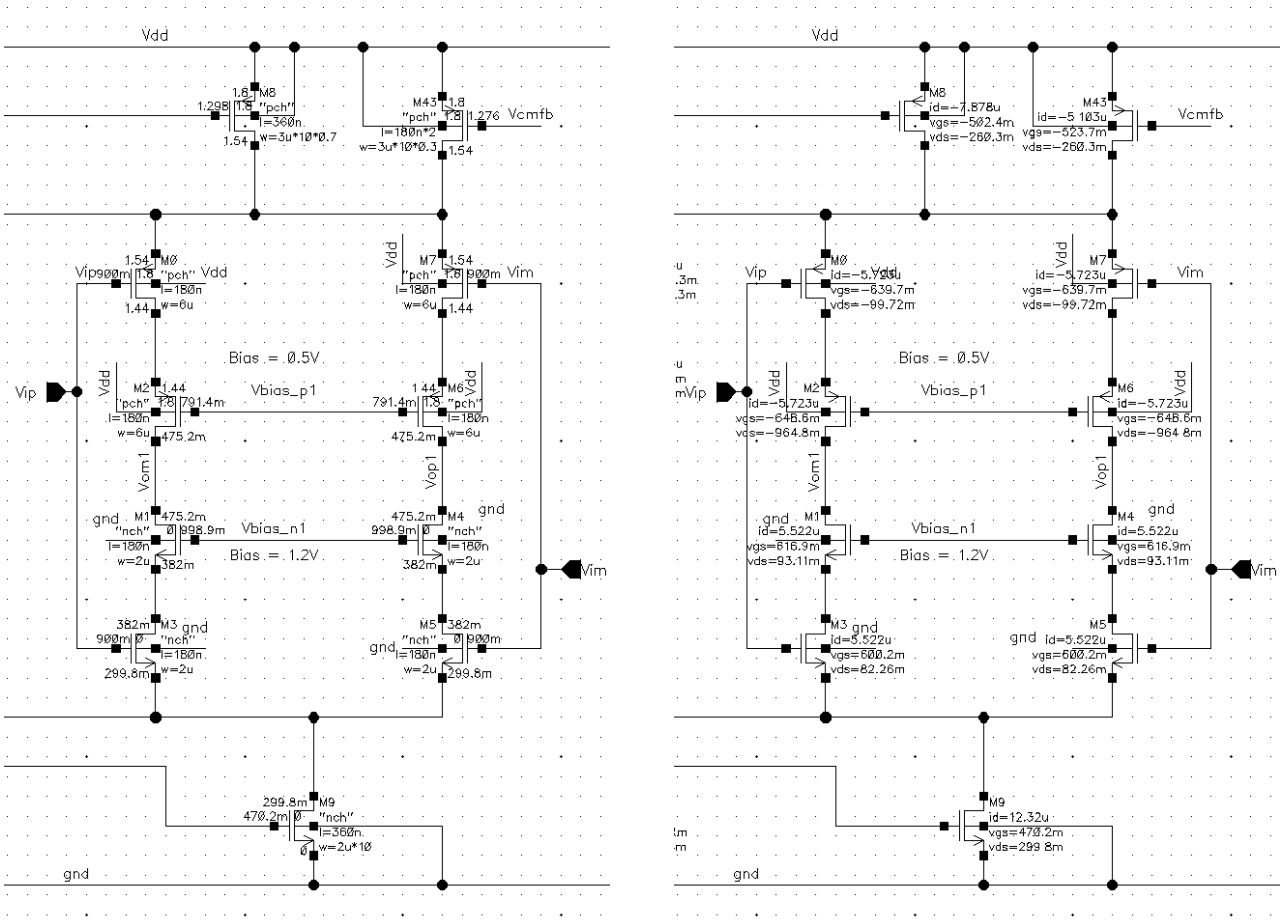
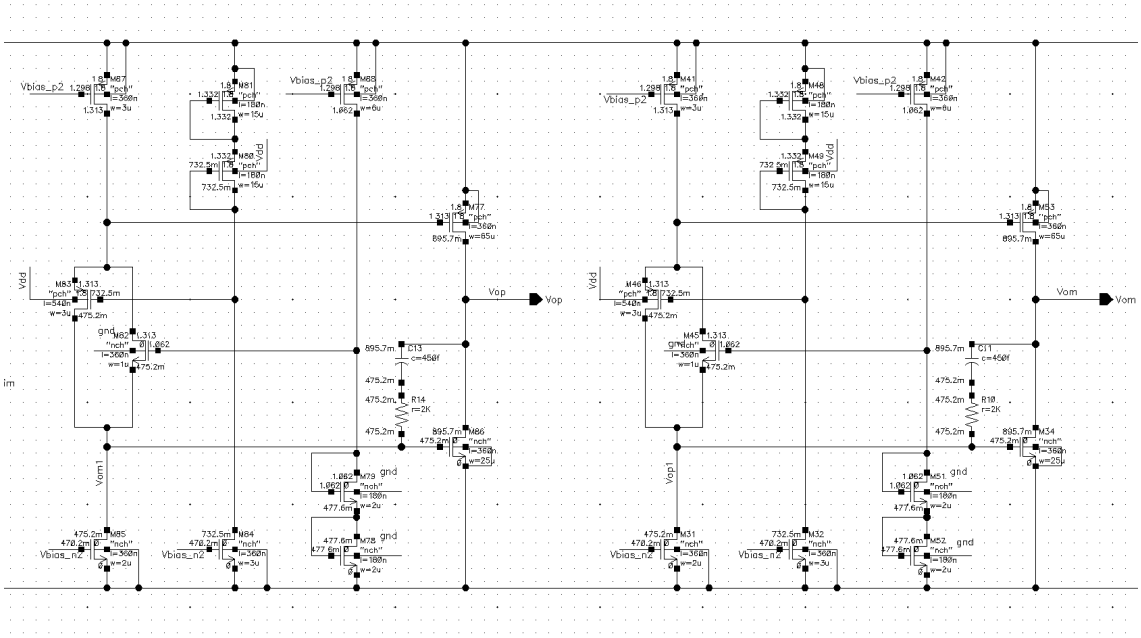
APPENDIX

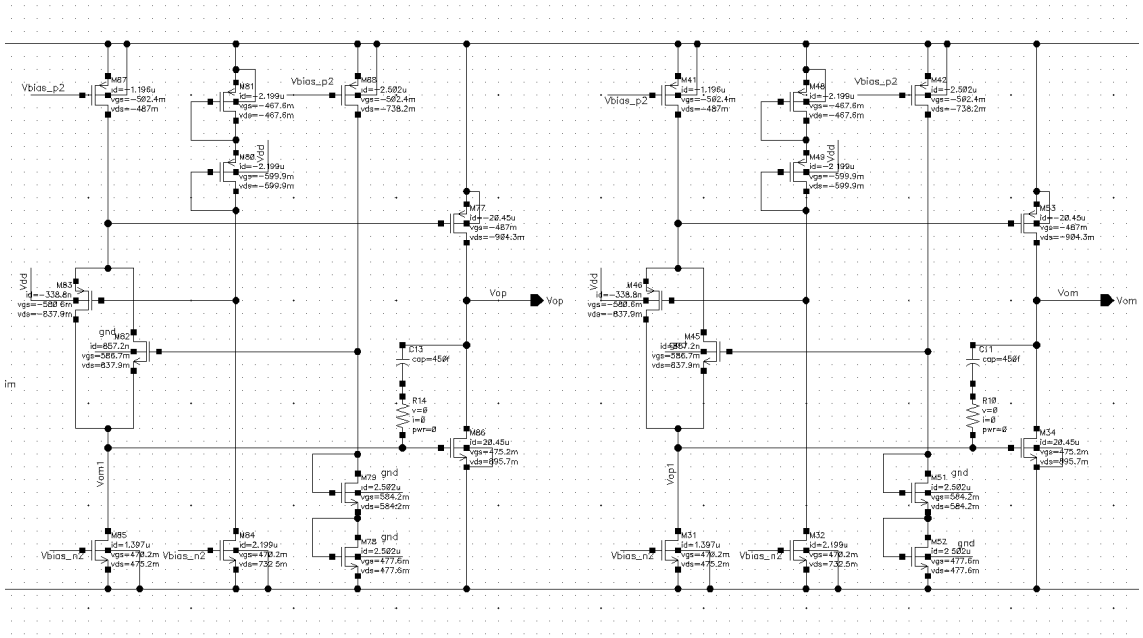


(a) (b)

Fig. 6: Schematic of first-stage amplifier with (a) size and (b) DC operating point.

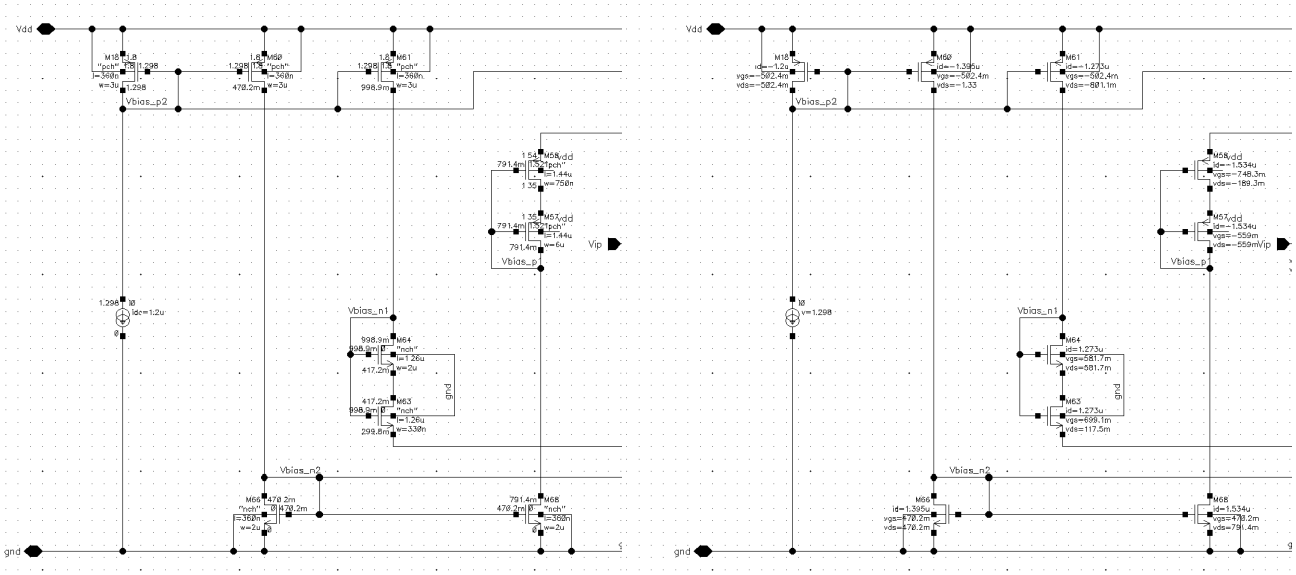


(a)



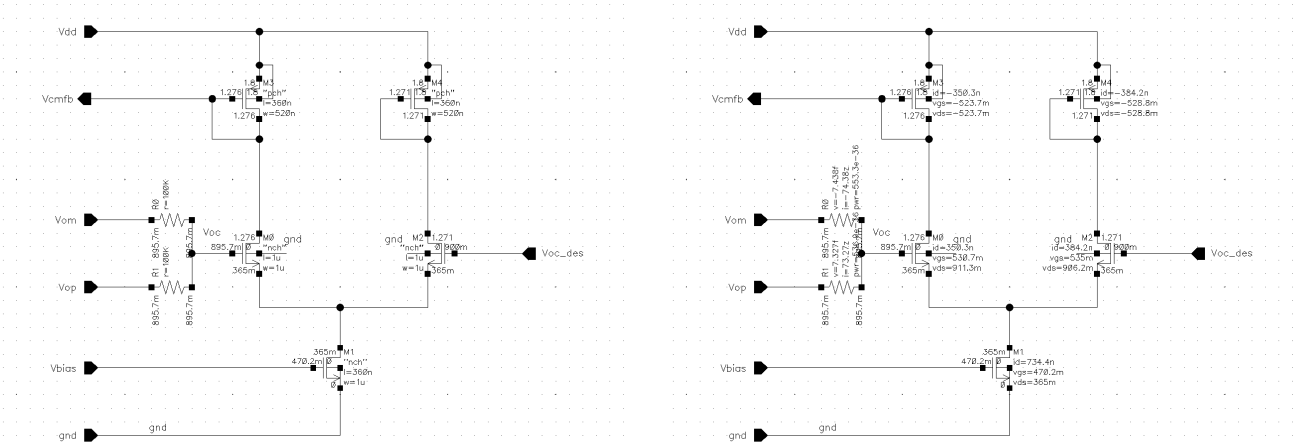
(b)

Fig. 7: Schematic of second-stage amplifier with (a) size and (b) DC operating point.



(a) (b)

Fig. 8: Schematic of biasing circuit with (a) size and (b) DC operating point.



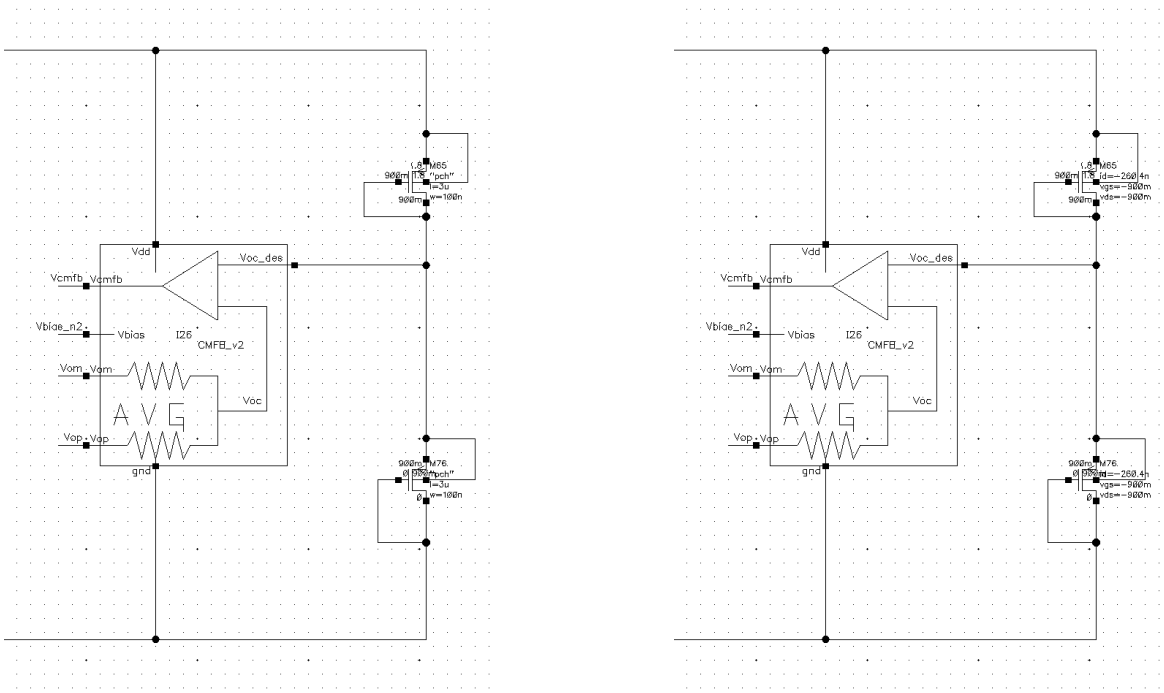


Fig. 9: Schematic of CMFB circuit with size and DC operating point.

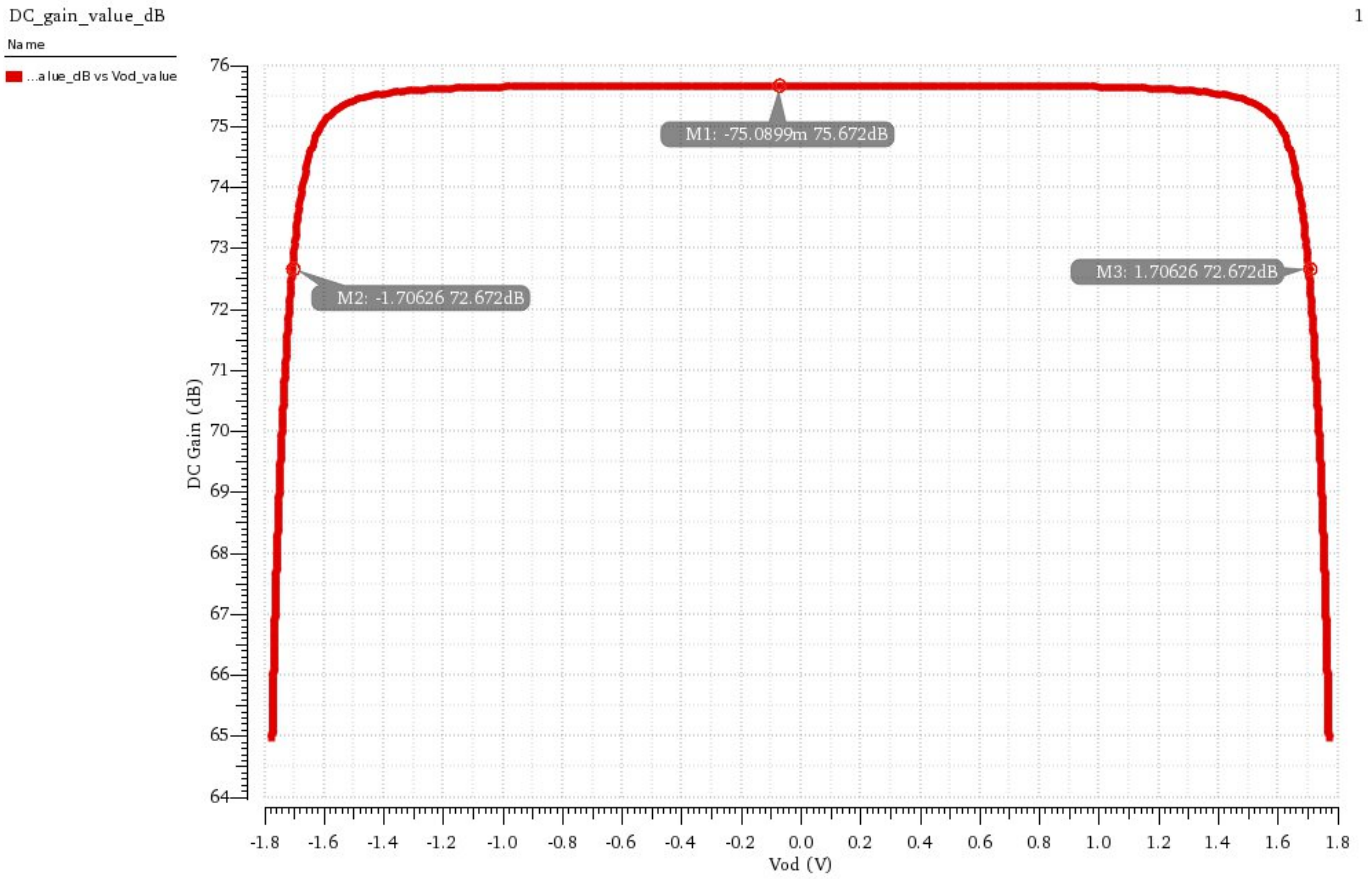


Fig. 10: DC gain versus output swing.

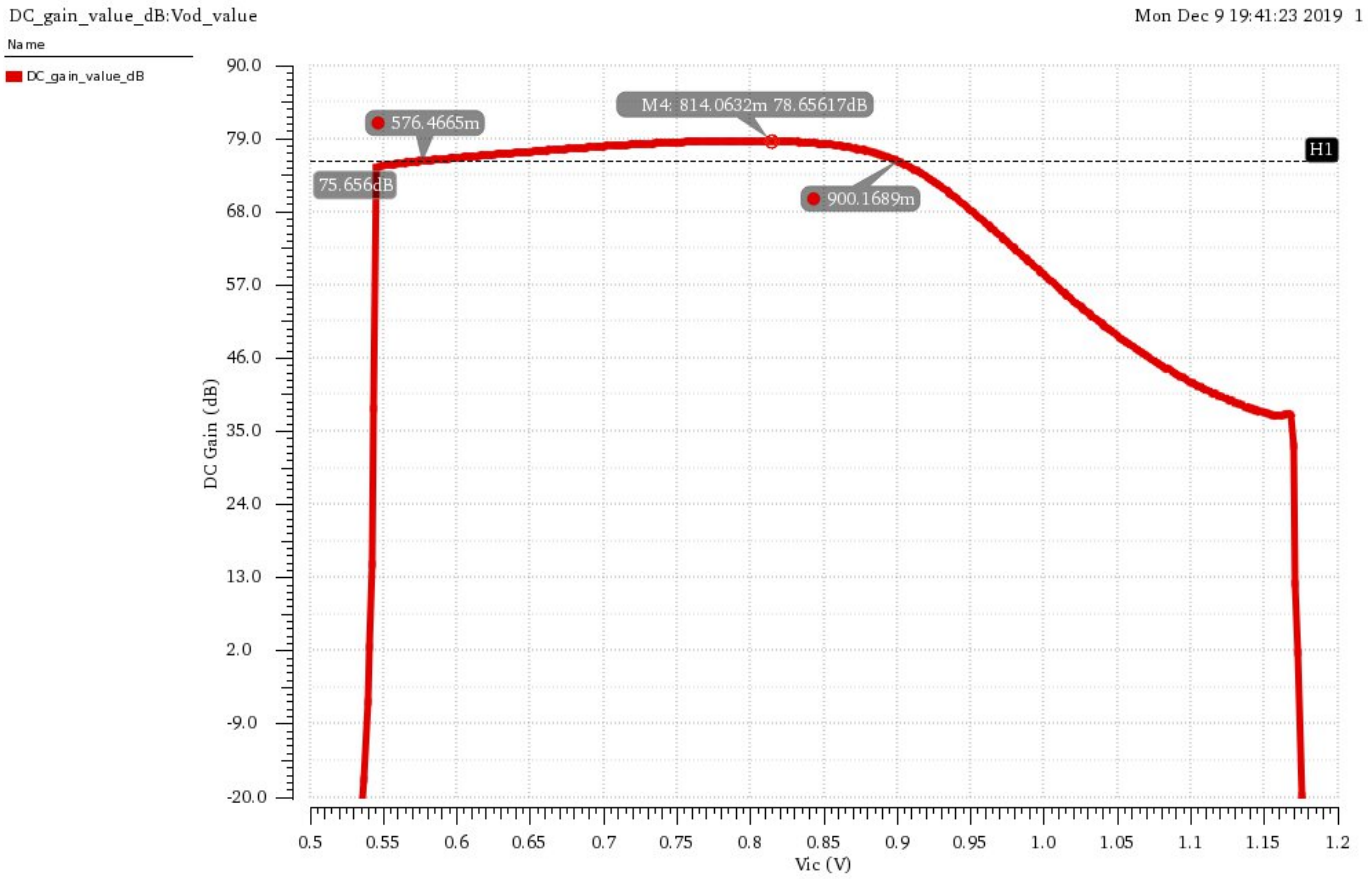


Fig. 11: DC gain versus output common-mode voltage.

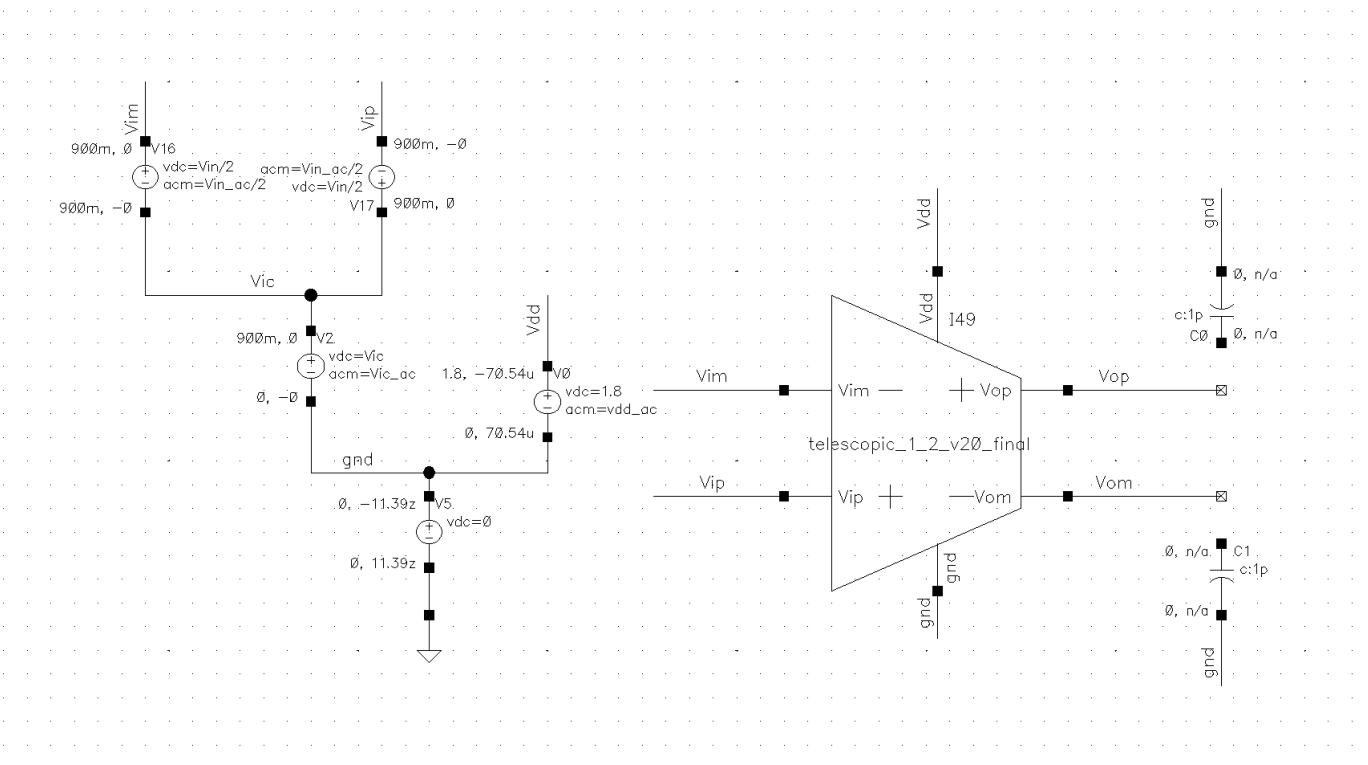


Fig. 12: Power consumption of the OTA.

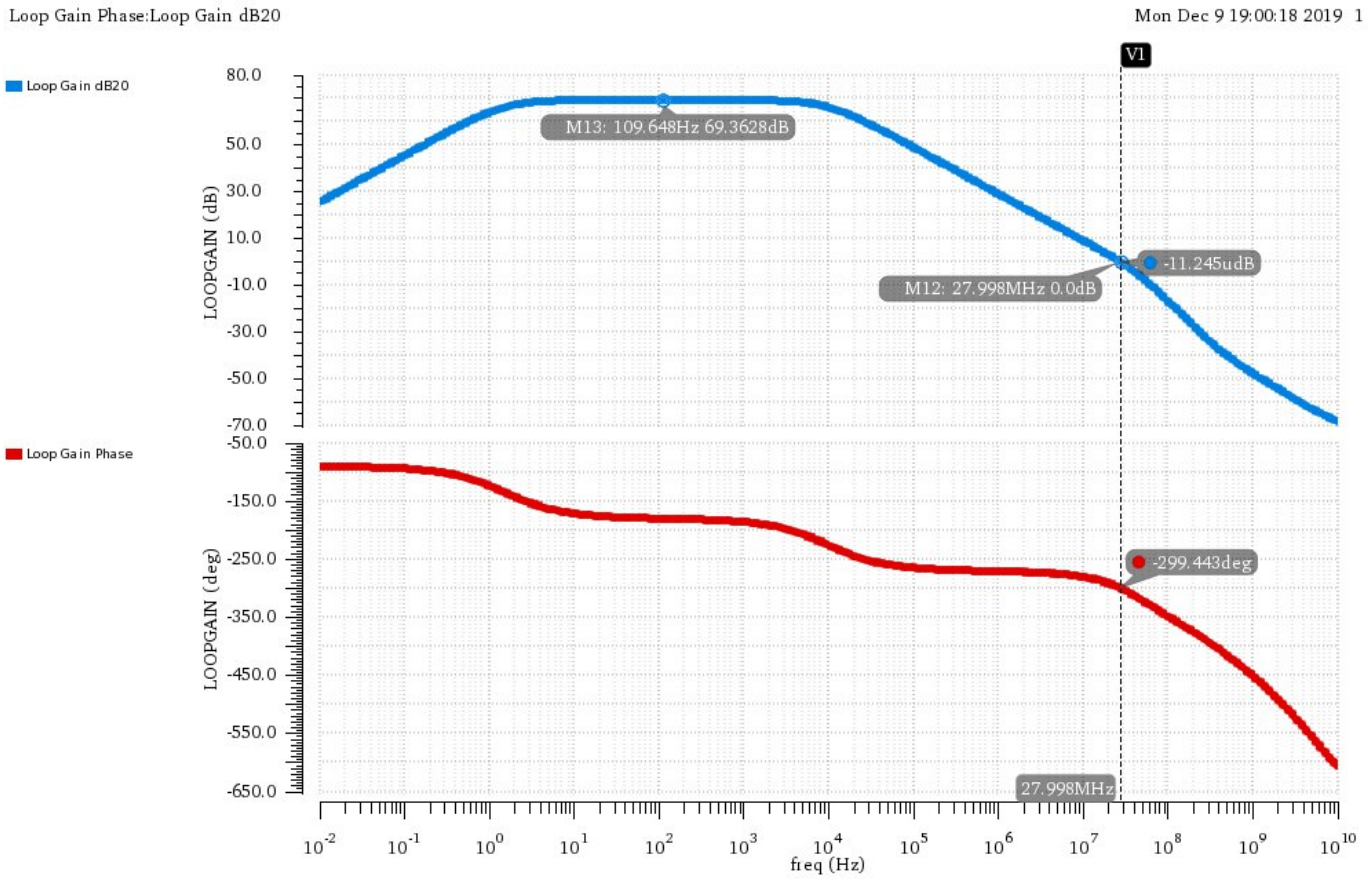


Fig. 13: Loop gain and phase margin.

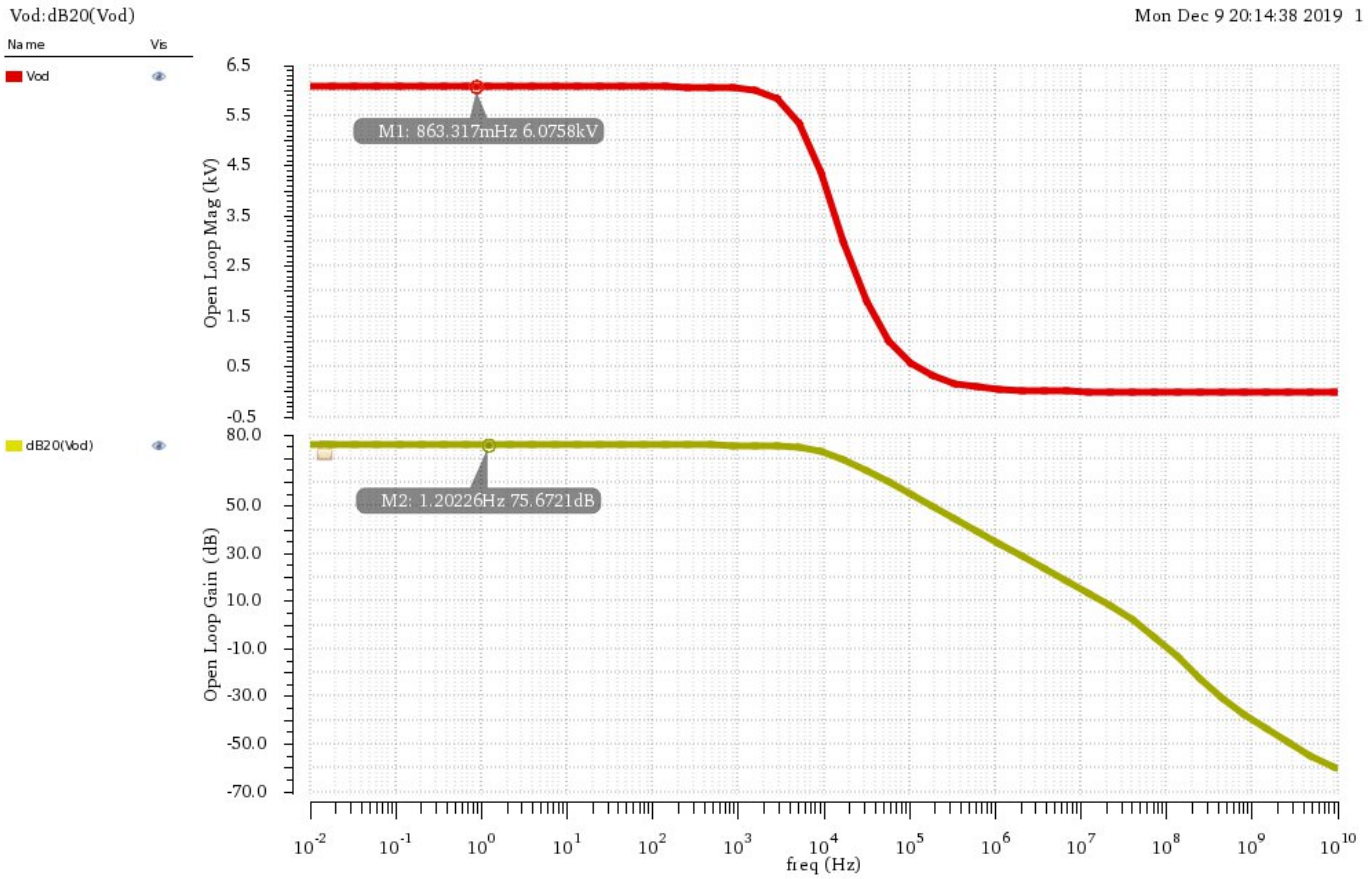
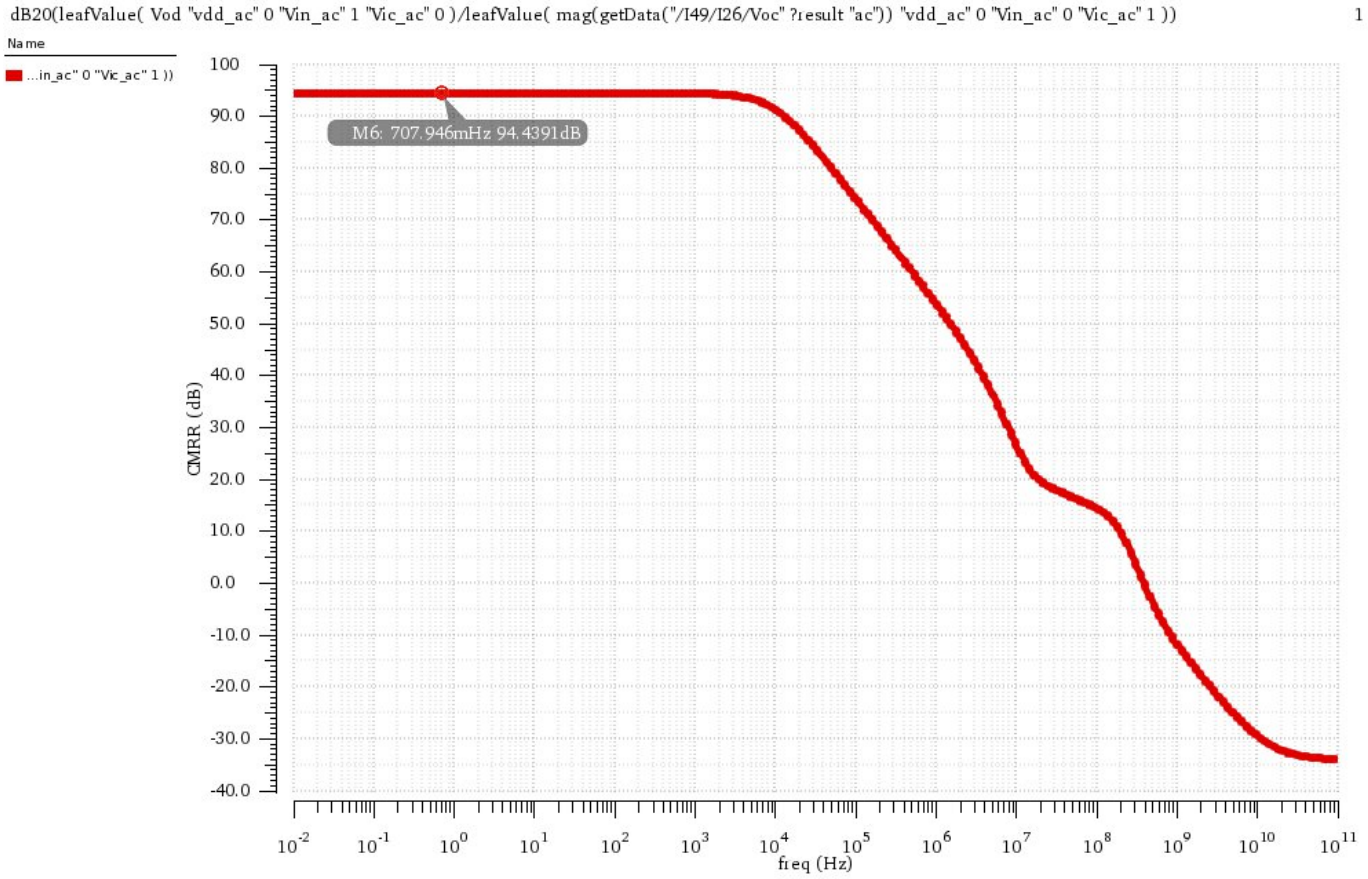


Fig. 14: Open loop gain magnitude and in dB.



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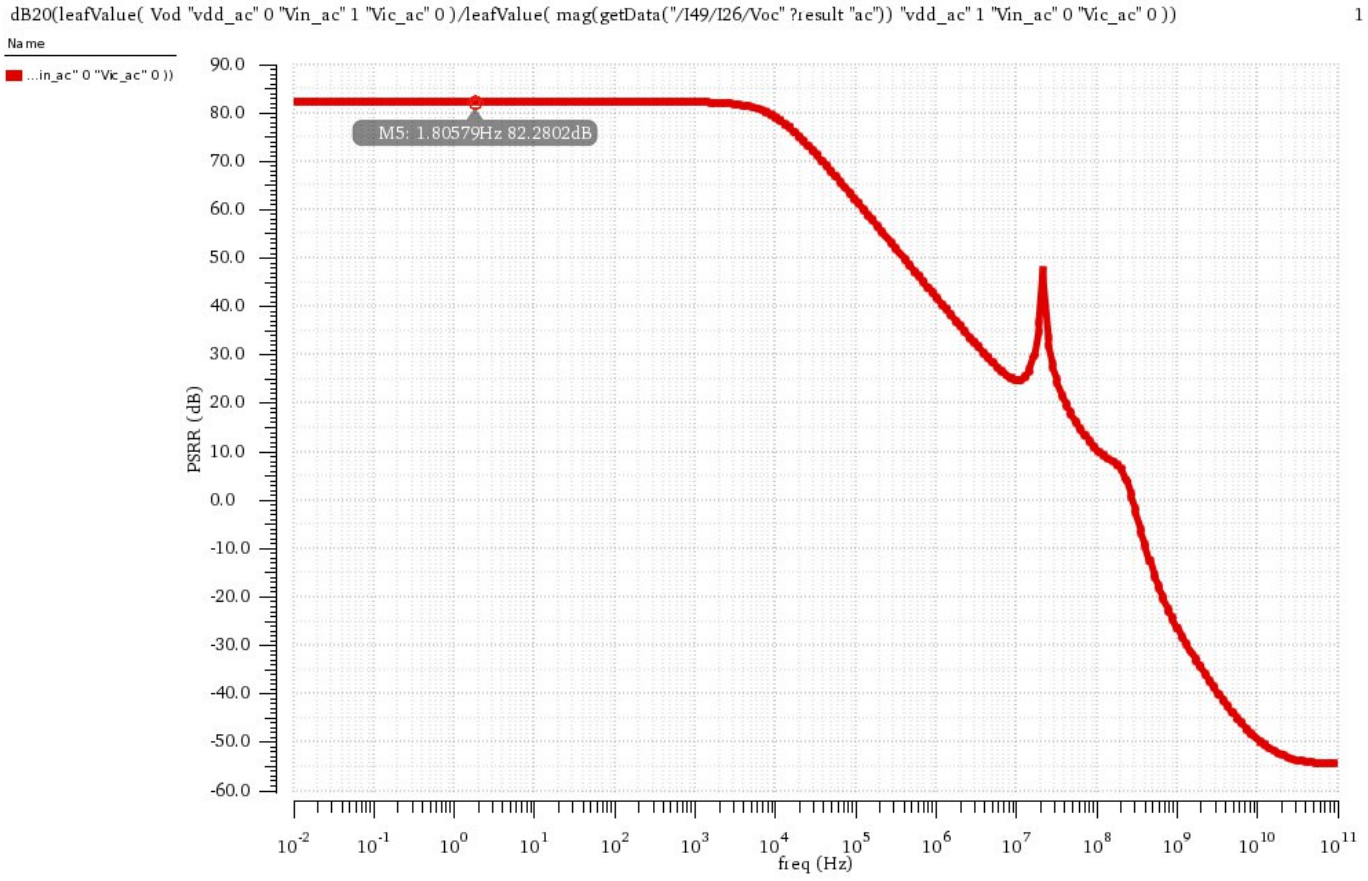


(b)

Fig. 15: (a) CMRR versus frequency; (b) PSRR versus frequency.

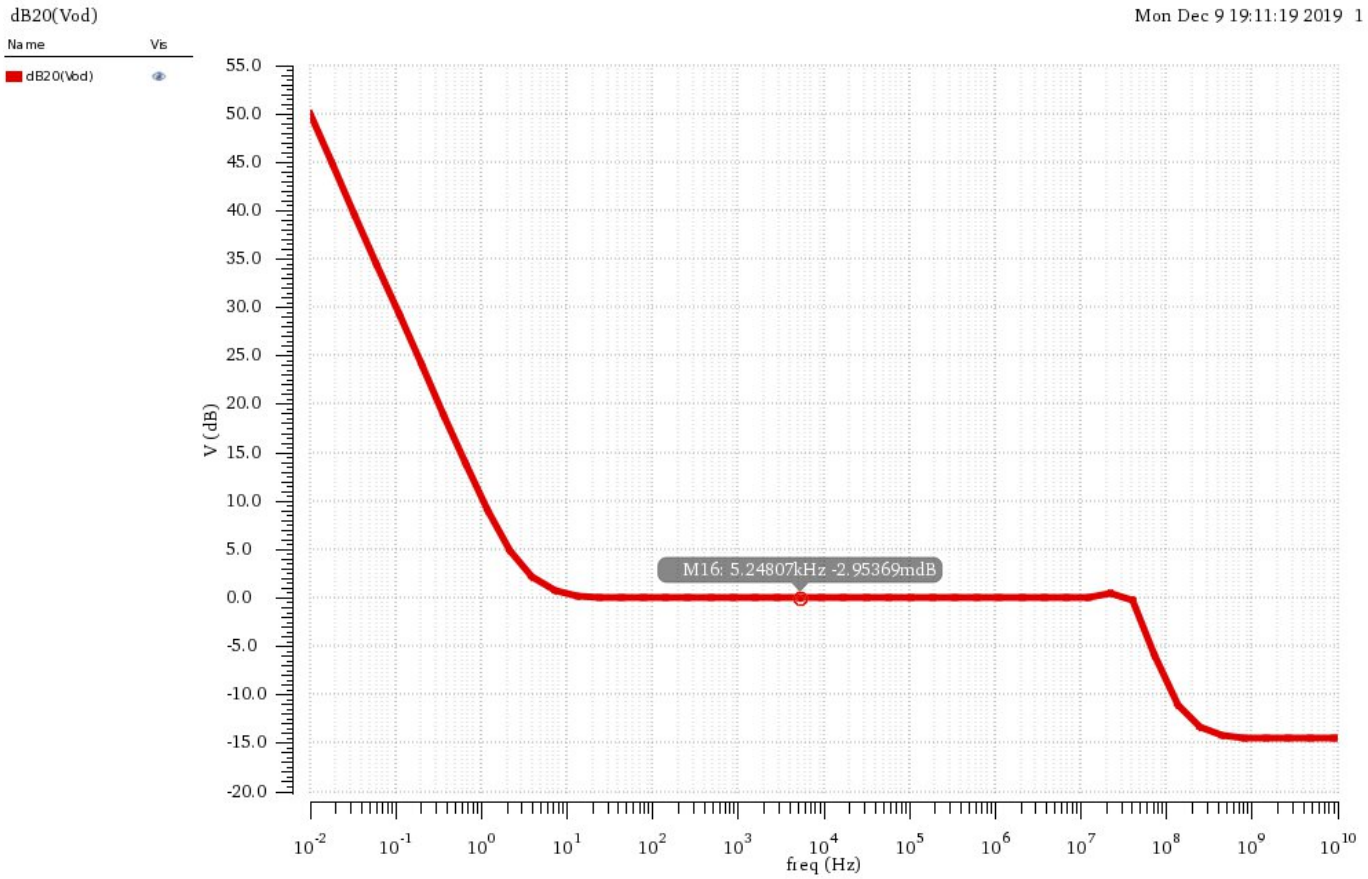
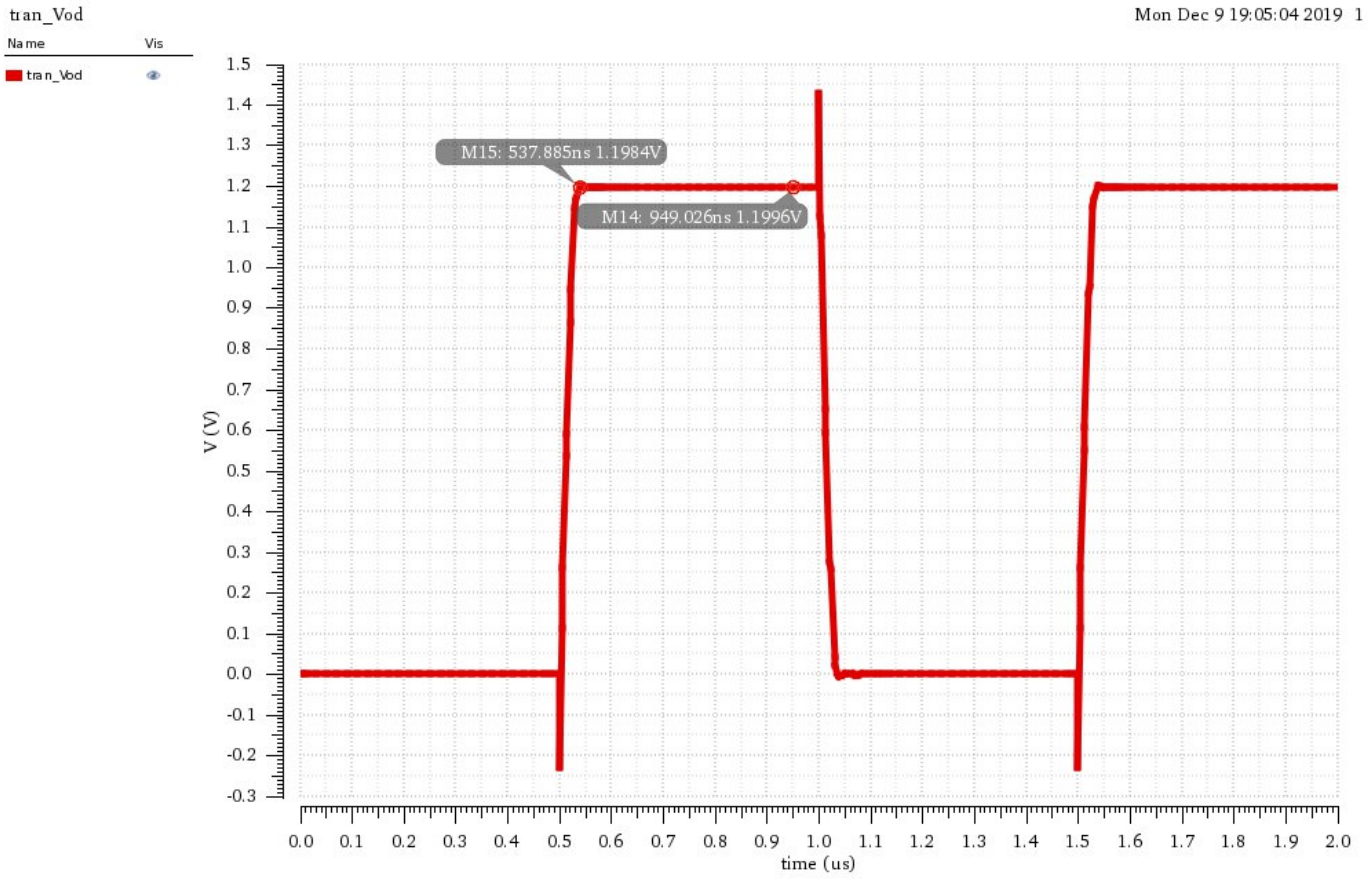


Fig. 16: OTA closed-loop frequency response.



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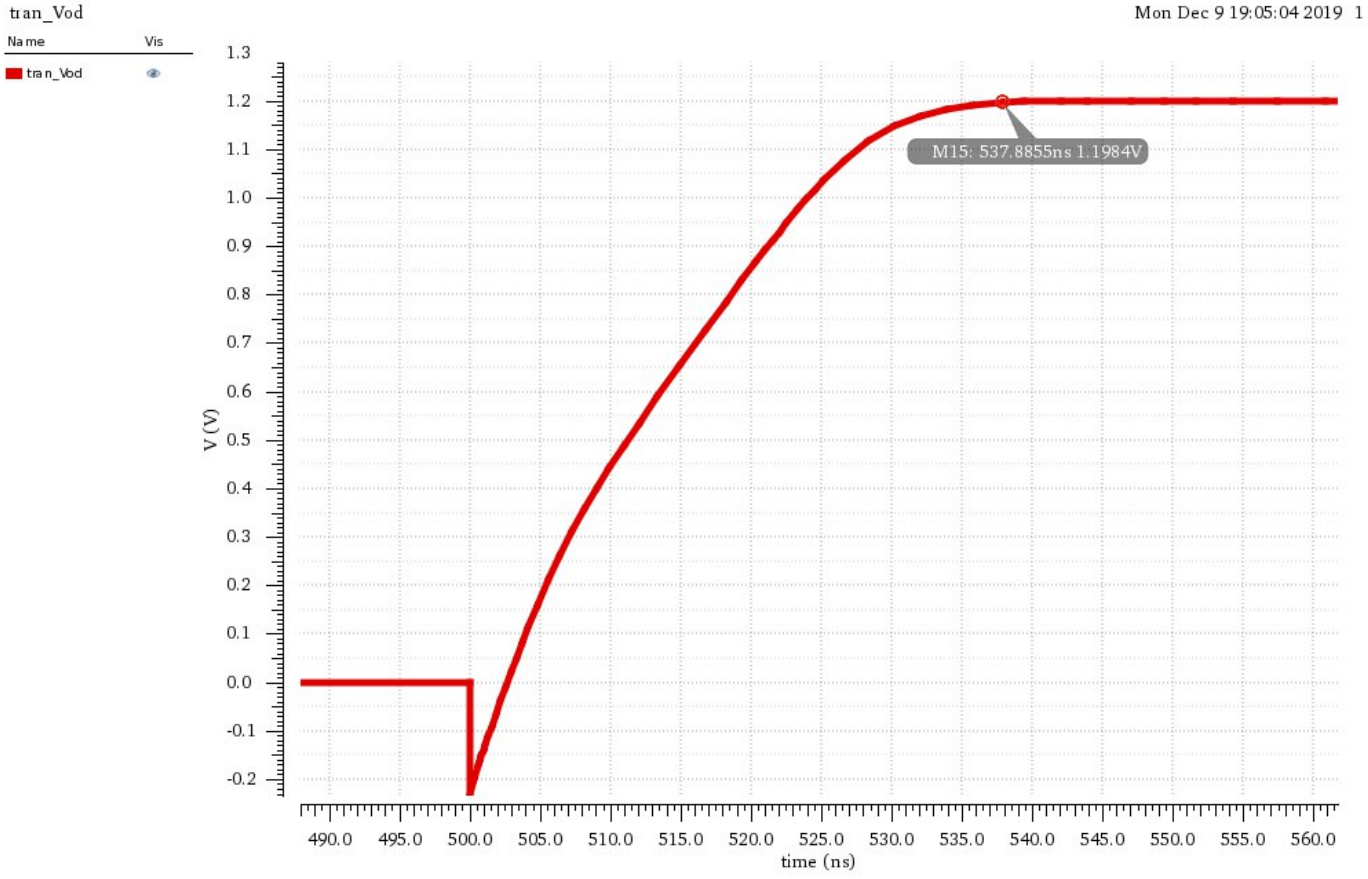
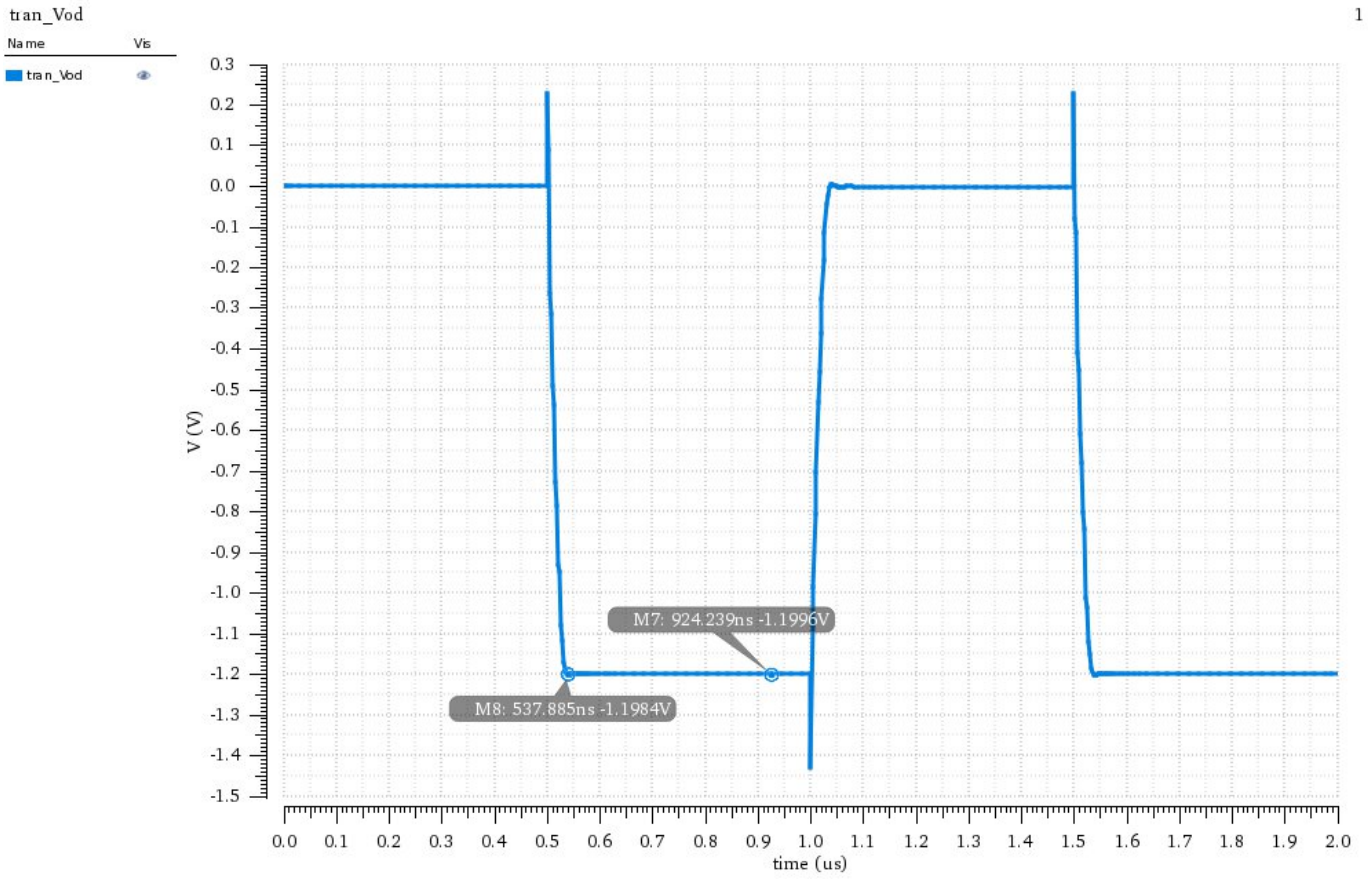


(b)

Fig. 17: (a) Settling (going up); (b) Zoomed-in waveform of (a).



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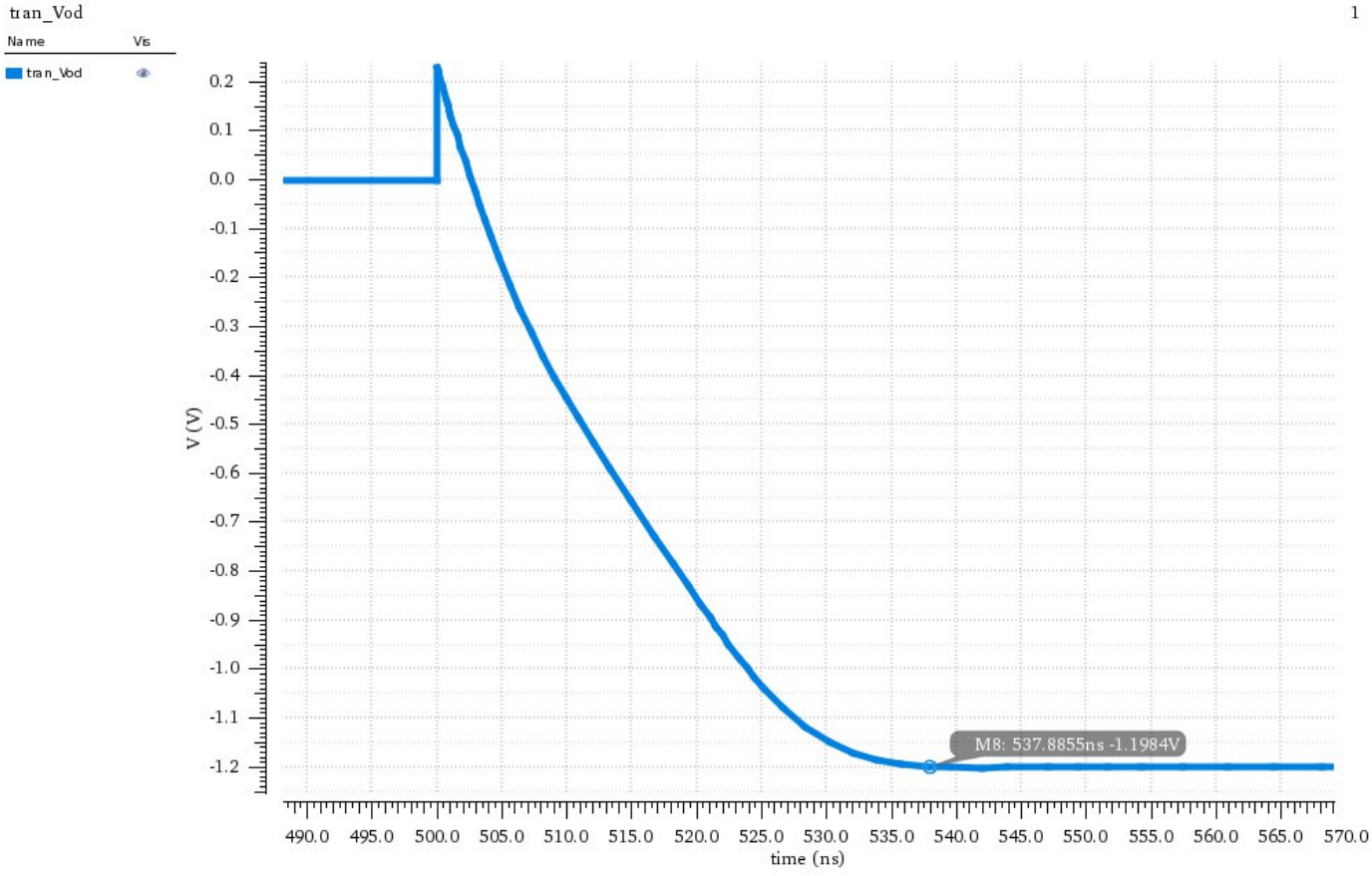

(b)

Fig. 18: (a) Settling (going down); (b) Zoomed-in waveform of (a).

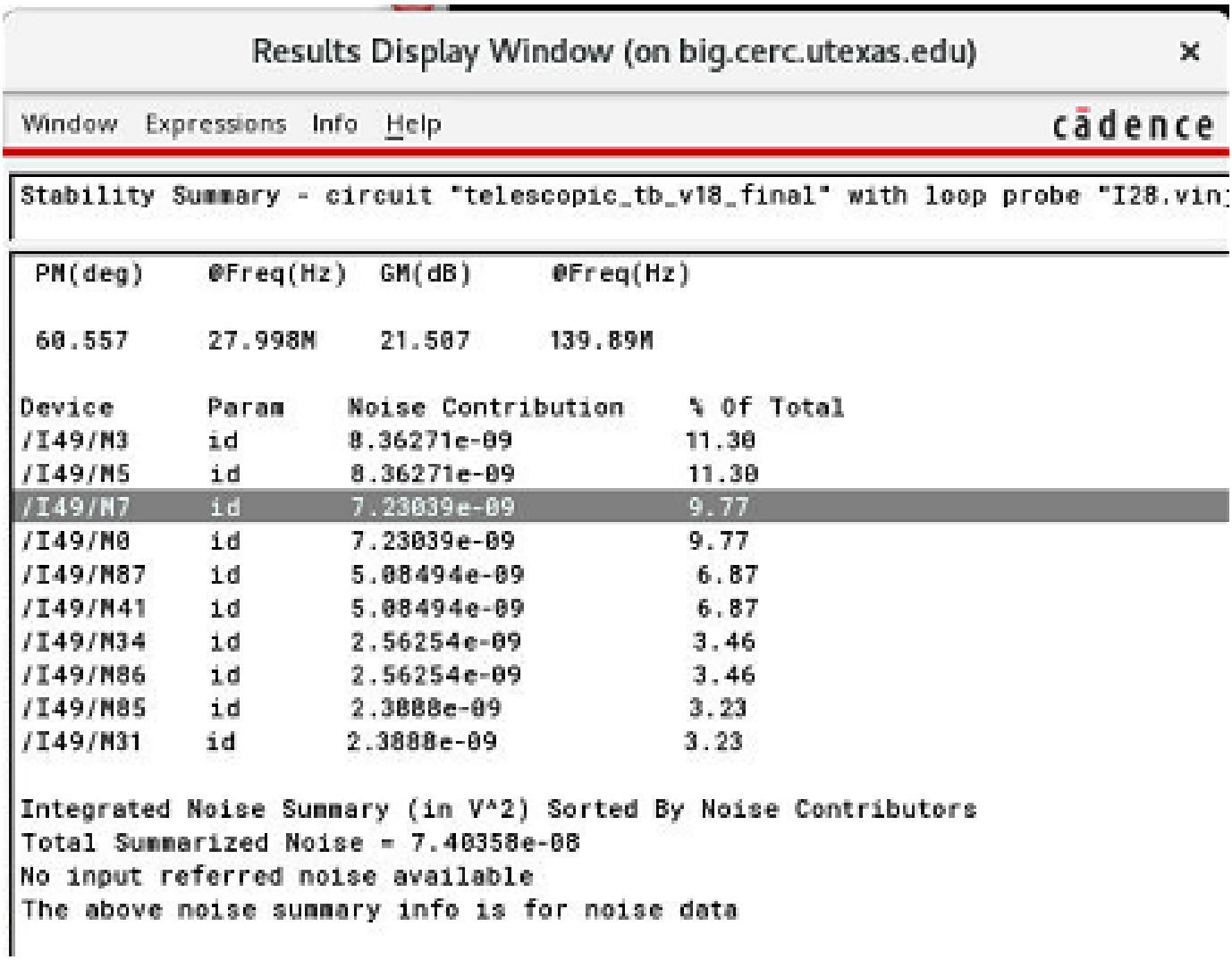

Fig. 19: Stability and noise summary.